REMARKS

Claims 1-4 are all the claims pending in the application. Claim 4 has been added to further define the invention. Please note that this Amendment has been formatted according to the Revised Format Now Permitted and, therefore, waiver of 37 C.F.R. § 1.121 is requested.[1] Reconsideration and allowance of all the claims are respectfully requested in view of the following remarks.

Claim Rejections - 35 U.S.C. § 103

The Examiner rejected claims 1-3 under §103(a) as being unpatentable over US Patent 6,193,132 to Shibata et al. (hereinafter Shibata) in view of US Patent 5,803,341 to Abe (hereinafter Abe) or JP 6-69286 (hereinafter JP '286). Applicants respectfully traverse this rejection because the references fail to teach or suggest all the elements as set forth and arranged in Applicants' claims.

Claim 1 sets forth, among other things, a chip recognition camera disposed to be lower than a level of a substrate mounted surface of a substrate stage, and that a substrate recognition camera is disposed above the substrate stage to recognize the substrate mounted on the substrate stage, and further wherein the chip and the substrate are subjected to positioning on the basis of recognition results of the chip recognition camera and the substrate recognition camera. These features are not taught or suggested by the prior art.

In particular, Shibata teaches that a chip 13 is recognized by the first recognition camera 14 from below, and then the bonded chip 13 is recognized by the second recognition camera 16. Additionally, Abe teaches that an LCD 1 and chip 2 are recognized by a single camera 4. This structure can recognize the chip through a transparent substrate such as LCD, but it cannot apply to the apparatus where an ordinary substrate (non-transparent) is mounted or a substrate is entirely mounted over the stage. Thus, neither Shibata nor Abe, when either taken alone or in combination, teaches or suggests the subject matter of claim 1.

[1] See Pre-OG Notices as posted on the PTO website at www.uspto.gov/web/offices/pac/dapp/opla/preognotice/revamdtprac.htm.

For at least the above reasons, claim 1 is not rendered obvious by Shibata, Abe, and JP '286. Likewise, dependent claims 2 and 3 are not rendered obvious by these references. However, Applicants traverse this rejection as it applies to claim 3 for the following additional reasons.

Claim 3 sets forth a bonding apparatus comprising: a bonding tool for holding a chip; a substrate stage for mounting a substrate; a moving mechanism for moving the bonding tool and the substrate stage relatively to each other; a chip recognition camera disposed lower than a level of a substrate mounted surface of the substrate stage to thereby recognize the chip held by the bonding tool so that the chip and the substrate are subjected to positioning on the basis of a recognition result of the chip recognition camera, wherein a lower surface of the chip is recognized by the chip recognition camera when the lower surface of the chip is located substantially on a level with a chip bonding surface of the substrate; and a chip tray for receiving the chip, the chip tray being located lower than the level of the chip bonding surface of the substrate.

Because the chip tray 12 is in a position lower than the level of the chip bonding surface of the substrate 3, the bonding tool 2 may be moved up to the level of the bonding surface after the chip bonding tool 2 has sucked the chip from the chip tray. In this case, the operation for moving the bonding tool is simplified.[2]

In contrast to that set forth in claim 3, none of the references applied by the Examiner even teaches or suggests a chip source at all, let alone its position with respect to the level of the chip bonding surface of the substrate. Instead, the Examiner makes the bald assertion that it would have been obvious to one of ordinary skill to provide a chip tray, "since the bonding tool needs to pick up the chip from a source. Therefore, having a chip tray would have been inherent to the apparatus to carry out the process."[3] However, even assuming that Shibata, Abe and JP

[2] Specification at paragraph 23.

[3] Office Action at page 3, last paragraph.

'286 taken together provide for some sort of chip source, there is still no motivation for positioning that chip source in the location as set forth in claim 3. That is, for the sake of argument, even assuming that Shibata, Abe, or JP '286 suggested a chip source, they do not teach or suggest any particular location of the chip source, let alone that it would be lower than a level of a chip bonding surface of a substrate, as set forth in claim 3.

For at least any of the above reasons, Shibata, Abe, and JP '286 fail to render obvious claim 3.

Conclusion

Claim 4 has been added to further define the invention. Claim 4 sets forth a bonding apparatus comprising: a bonding tool for holding a chip; a substrate stage for mounting a substrate; and a chip recognition camera disposed lower than a level of a substrate mounted surface of the substrate stage to thereby recognize the chip held by the bonding tool, wherein a lower surface of the chip is recognized by the chip recognition camera when the lower surface of the chip is located within ± 5 mm of a plane in which is located a chip bonding surface of the substrate.

For example, as shown in Figs. 1 and 2A, a chip bonding apparatus comprises: a bonding tool 2 for holding a chip 1; a substrate stage 4 for mounting a substrate 3; and a chip recognition camera 11 disposed lower than a level of a substrate mounted surface of the substrate stage 4 to thereby recognize the chip 1 held by the bonding tool 2, wherein a lower surface of the chip 1 is recognized by the chip recognition camera 11 when the lower surface of the chip 1 is located within ± 5 mm of a plane in which is located a chip bonding surface of the substrate 3.

As discussed in paragraphs 3 and 4 of the present specification, when the constituent members of a bonding tool age, the accuracy in positioning of a chip with respect to a substrate deteriorates so that there is a deviation between the position of the chip and the desired position of the chip. The deviation in position is due at least in part to the fact that in the prior art, the chip is image recognized at a position higher than the level of the chip bonding surface of the substrate. See also Figs. 3A and 3B.

According to the arrangement of claim 4, however, because the image recognition of the chip is performed in the position where the substrate 3 and chip 1 should be bonded to each other, the substrate 3 and chip 11 can be bonded accurately without deviation.[4] That is, the deviation will not be larger than 1 μm because the error between the level of the lower surface of the chip 1 and the level of the chip bonding surface of the substrate 3 at the time of the image recognition is within ± 5 mm.[5]

In contrast to that set forth in claim 4, Shibata, Abe, and JP '286 do not teach or suggest a bonding apparatus wherein the lower surface of the chip is positioned within ± 5 mm of a plane in which is located a chip bonding surface of a substrate.

Shibata teaches that the camera 14 recognizes an image on the chip 13 when the chip is at a position significantly higher than the chip bonding surface of substrate 11. See Fig. 5, wherein the relative positions of the chip 13 and substrate 1 are shown.

Abe discloses that the positioning object 18 on the TCP 17 is brought within the focussing range A of the camera 4 so as to be image recognized thereby. However, Abe fails to teach or suggest that the positioning object 18 is within ± 5 mm of a plane in which is located the bonding surface of LCD 1. See, for example, Fig. 2 wherein Abe shows but does not quantify the positional relationship between TCP 17 and LCD 1 when the camera 4 images the positioning object 18.

Lastly, JP '286 teaches that a camera 10 is used below a transparent substrate 14 to more accurately position a photodiode element 15 with respect to the substrate 14. In paragraph 9, JP '286 teaches that the photodiode element 15 and the silicon on sapphire 14 are made to approach, and the camera 10 is then used to assist in alignment.[6] However, JP '286 fails to teach or suggest

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[4] Specification at paragraphs 21 and 24.

[5] Specification at paragraph 22.

[6] This teaching comes from a computer translation of JP '286, a copy of which is provided herewith for the Examiner's convenience.

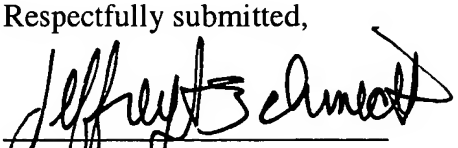
how close element 15 is to the bonding face of the substrate 14 when the alignment occurs. Accordingly, JP '286 fails to teach or suggest that a lower surface of a chip is recognized by a chip recognition camera when the lower surface of the chip is located within ± 5 mm of a plane in which is located a chip bonding surface of the substrate, as set forth in claim 1.

Therefore, for the sake of argument, even assuming that one of ordinary skill in the art were motivated to combine Shibata with Abe or JP '286 as suggested by the Examiner, any such combination would still not teach or suggest that a lower surface of a chip is recognized by a chip recognition camera when the lower surface of the chip is located within ± 5 mm of a plane in which is located a chip bonding surface of the substrate, as set forth in claim 4.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the mounting method of semiconductor parts and electronic parts.
[0002]
[Description of the Prior Art] The example of conventional flip-chip-bonding equipment is shown in drawing 1 .
[0003] The semiconductor parts 6 adsorbed by the vacuum collet 1 moving up and down perform alignment under a microscope 2 through a one-way mirror 3, and are heating and carrying out bonding of the polar zone of the semiconductor parts 6, and the polar zone of the mounting substrate 7 by the susceptor 4. In this case, since the one-way mirror 3 is minded in order to see the electrode of the semiconductor parts 6, the mounting substrate 7 and a certain amount of interval are needed, and since alignment is made only where an interval is taken, alignment precision is set to about **20 micrometers. Such technology is expressed to the volume "hybrid integrated circuit" **** and on thick ruble, and Kogyo Chosakai Publishing Co., Ltd. (October, 1968) in detail.
[0004]
[Problem(s) to be Solved by the Invention] By the conventional method, since alignment was performed in the flip chip using the one-way mirror, there was the following problem.
1. Alignment precision was as large as **20 micrometers, and the increase in capacity by position gap and the problem which detailed electrodes contact arose.
2. The wettability of solder could not be checked, but it heated too much and the faulty connection by the assembly produced breakage of ** and the semiconductor parts of a load twisted for hanging too much etc.
3. Parallelism adjustment could not be detected but per a position gap and piece of semiconductor parts etc. arose.
4. The oxide film arose on the solder layer front face during heating of semiconductor parts and alignment, it became factors, such as an adhesive strength fall, and the problem to which reliability falls arose.
5. By the rear-face accepting-reality doubling method using transparent sub mounting, the chip was fixed and heated, it was a sub mounting side, and in order to perform doubling, there was a problem that much flip chip bonding of a chip was not made.
[0005] The purpose of this invention is to solve the above-mentioned trouble.
[0006]
[Means for Solving the Problem] The above-mentioned purpose is solved by the means shown below.
1. Perform and carry out bonding of heating and the pressurization from an opposite side, observing the plane of composition of a mounting device with a microscope or a television camera from a substrate rear face using a substrate with high permeability on the light or specific wavelength.
2. Prepare the parallelism controller of a bonding area material side in a stage side.

3. Either a semiconductor-device side or a substrate side prepares the function in which a scrub or an ultrasonic wave is imposed.
4. Transparence-ize a substrate and prepare the function which adsorbs a semiconductor device by the collet which has a heating mechanism, and is made into working.
[0007]
[Function] 1. Since the plane of composition of a mounting device is observable from a substrate rear face, the alignment precision of **2 micrometers or less can be attained, and the wettability of solder can be checked.
2. Since the degree adjustment of parallel is detectable, per pieces, such as semiconductor parts, can be prevented.
3. Since it has the function in which a scrub or an ultrasonic wave is imposed, the oxide film on the front face of solder is removable.
4. Many semiconductor devices can be mounted by flip chip bonding by preparing the function which transparence-izes a substrate, adsorbs by the collet which has a heating mechanism, and is made into working.
[0008]
[Example] The example of this invention is explained using a drawing below.
[0009] The example used sapphire (10mm angle x0.2mm **) as a transparent substrate in mounting of a front end module, as shown in drawing 2 . Wiring was formed in the front face of silicon on sapphire 14 using thin film Ti/Pt/Au (0.1 / 0.2/0.9mm **). Moreover, it is made smaller 2 micrometers than the electrode pattern of an element, and the pattern of the joint for joining a photodiode 15 is about 3-micrometer thick ****** about the solder of Pb/Sn (95/5) on it. First, silicon on sapphire 14 is fixed on a susceptor 4, and the photodiode element 15 is adsorbed by the vacuum collet 1. The microscope 2 attached in the collet side performs rough alignment. The vacuum collet 1 is lowered and the photodiode element 15 and silicon on sapphire 14 are made to approach. From the camera 10 arranged at the rear-face side of silicon on sapphire 14, alignment of the joint of silicon on sapphire 14 and the photodiode element 15 is performed using the jogging stage 5, the Z-axis stage 8, and the influence stage 9. A scrub is applied to the vacuum collet 1 by the scrub mechanism 11, carrying out solder fusion at 340 degrees C, after exact alignment is completed, the oxide film on the front face of solder is removed, and junction by intrinsic solder is completed.
[0010]
[Effect of the Invention] 1. Since the plane of composition of a mounting device was observable from a substrate rear face, the alignment precision of **2 micrometers or less has been attained.
2. Since the degree adjustment of parallel was detectable, per pieces, such as semiconductor parts, was able to be prevented.
3. Since it had the function in which a scrub or an ultrasonic wave is imposed, the oxide film on the front face of solder could be removed, and the wettability of solder was able to be checked.
4. Many semiconductor devices were able to be mounted by flip chip bonding by preparing the function which transparence-izes a substrate, adsorbs by the collet which has a heating mechanism, and is made into working.

[Translation done.]